METHODOLOGY AND APPLICATIONS OF TIMING-DRIVEN LOGIC RESYNTHESIS FOR VLSI CIRCUITS

Background of the Invention

Field of the Invention

[0001] Aspects of the present invention generally relate to computer aided engineering of logic circuits. More particularly, embodiments of the present invention relate to timing optimization of logic circuits.

Description of the Related Technology

[0002] In a programmable interconnect-based cluster (PIC), a group of basic logic blocks are connected by a local programmable interconnection array that usually provides full connectivity and is much faster than global or semi-global programmable interconnects. A number of commercial PLDs use the PIC architecture, such as the logic array block (LAB) in Altera FLEX 10K and APEX 20K devices, and the MegaLAB in APEX 20K devices. For example, in FLEX 10K devices, each LAB consists of eight 4-LUTs connected by the local interconnect array. Multi-level hierarchy can be formed easily using PICs, in which a group of small (lower-level) PICs may be connected through a programmable interconnect array at this level to form a larger (higher-level) PIC. For example, in Altera APEX 20K FPGAs, each LAB consists of ten 4-LUTs connected by local interconnects, which forms the first-level PIC. Then, 16 such LABs, together with one embedded system block and another level of programmable interconnects, form a second level PIC, called MegaLAB. Finally, global interconnects are used to route between MegaLAB structures and to I/O pins.

[0003] As timing problems become more and more crucial in integrated circuit (IC) designs, timing-driven logic resynthesis is often needed at various design stages to minimize circuit delays. Timing-driven logic resynthesis is usually conducted using an iterative refinement-based approach on a critical netlist due to a potential area penalty associated with the local transformations for delay reduction. In each pass (or iteration), an overall circuit delay target that is smaller than the current maximum arrival time is set, and a set of local transformations are selected to meet this delay target. If the delay target is met,